AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method to facilitate cache coherence with adaptive write updates, comprising:

initializing a cache to operate using a write-invalidate protocol, wherein this initializing is performed by a cache controller residing in a processor;

monitoring a dynamic behavior of the cache during program execution, wherein monitoring the dynamic behavior of the cache involves maintaining a count for each cache line of the number of cache line invalidations the cache line has been subject to during program execution, wherein this monitoring is performed by the cache controller in the processor; and

if the dynamic behavior indicates that better performance can be achieved using a write-broadcast protocol, switching the cache to operate using the write-broadcast protocol, wherein this switching is performed by the cache controller in the processor.

2 (Canceled).

3. (Currently amended) The method of ~~claim 2~~ claim 1, wherein switching to the write-broadcast protocol involves switching to the write-broadcast protocol on a cache-line by cache-line basis.

4 (Canceled).

5. (Previously presented) The method of claim 1, wherein if the number of cache line invalidations indicates that a given cache line is updated frequently, switching the cache line to operate under the write-broadcast protocol.

6. (Original) The method of claim 5, wherein if a given cache line is using the write-broadcast protocol and the number of cache line updates indicates that the given cache line is not being contended for by multiple processors, switching the given cache line back to the write-invalidate protocol.

7. (Currently amended) The method of claim 1, wherein if a shared memory multiprocessor includes ~~modules~~ caches that are not able to switch to the write-broadcast protocol, the method further comprises locking the cache into the write-invalidate protocol.

8. (Currently amended) The method of claim 1, wherein when a cache is operating under the write-invalidate protocol, ~~sends~~ an invalidation message is sent to other caches in a shared memory multiprocessor when a given cache line is updated in a local cache.

9. (Currently amended) The method of claim 1, wherein when a cache is operating under the write-broadcast protocol, ~~broadcasts~~ an update is broadcast to other caches in a shared memory multiprocessor when the given cache line is updated in a local cache.

10. (Currently amended) An apparatus to facilitate cache coherence with adaptive write updates, comprising:

an initializing mechanism configured to initialize a cache to a write-invalidate protocol, wherein the initializing mechanism is present in a cache controller in a processor;

an monitoring mechanism configured to monitor a dynamic behavior of the cache, wherein monitoring the dynamic behavior of the cache involves maintaining a count of cache line invalidations initiated by each processor within a shared memory multiprocessor, wherein the monitoring mechanism is present in the cache controller in the processor; and

a protocol switching mechanism configured to switch the cache to a write-broadcast protocol if the dynamic behavior indicates that better performance can be achieved using the write-broadcast protocol, wherein the protocol switching mechanism is present in the cache controller in the processor.

11 (Canceled).

12. (Currently amended) The apparatus of ~~claim 11~~ claim 10, wherein switching to the write-broadcast protocol involves switching to the write-broadcast protocol on a cache-line by cache-line basis.

13 (Canceled).

14. (Previously presented) The apparatus of claim 10, wherein if the count of cache line invalidations indicates that a given cache line is updated frequently in different caches of the shared memory multiprocessor, switching the cache to the write-broadcast protocol.

15. (Original) The apparatus of claim 14, wherein if the given cache line is using the write-broadcast protocol and the count of cache line invalidations

indicates that the given cache line is being invalidated in only one cache, switching the cache to the write-invalidate protocol.

16. (Currently amended) The apparatus of claim 10, further comprising a locking mechanism configured to lock the cache into the write-invalidate protocol if the shared memory multiprocessor includes ~~modules~~ caches that are not able to switch to the write-broadcast protocol.

17. (Currently amended) The apparatus of claim 10, wherein when the cache is operating under the write-invalidate protocol, ~~involves sending~~ an invalidate message is sent to other caches within a shared memory multiprocessor when a given cache is written to.

18. (Currently amended) The apparatus of claim 10, wherein when the cache is operating under the write-broadcast protocol, ~~involves broadcasting~~ a data update message is broadcast to other caches within a shared memory multiprocessor when a given cache is written to.

19. (Currently amended) A computing system that facilitates cache coherence with adaptive write updates, comprising:

a plurality of processors, wherein a processor within the plurality of processors includes a cache;

a shared memory;

a bus coupled between the plurality of processors and the shared memory, wherein the bus transports addresses and data between the shared memory and the plurality of processors

an initializing mechanism configured to initialize the cache to a write-invalidate protocol, wherein the initializing mechanism is present in a cache controller in a processor;

a monitoring mechanism configured to monitor a dynamic behavior of the cache, wherein monitoring the dynamic behavior of the cache involves maintaining a count of cache line invalidations initiated by each processor within a shared memory multiprocessor, wherein the monitoring mechanism is present in the cache controller in the processor; and

a protocol switching mechanism configured to switch the cache to a write-broadcast protocol if the dynamic behavior indicates that better performance can be achieved using the write-broadcast protocol, wherein the protocol switching mechanism is present in the cache controller in the processor.

20. (Currently amended) A means to facilitate cache coherence with adaptive write updates, comprising:

an initializing means for initializing a cache to a write-invalidate protocol, wherein the initializing means is present in a cache controller in a processor;

a monitoring means for monitoring a dynamic behavior of the cache, wherein monitoring the dynamic behavior of the cache involves monitoring the dynamic behavior of the cache on a cache-line by cache-line basis, wherein the monitoring means is present in the cache controller in the processor; and

a protocol switching means for switching the cache to a write-broadcast protocol if the dynamic behavior indicates that better performance can be achieved using the write-broadcast protocol, wherein the protocol switching means is present in the cache controller in the processor.